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ART UNIT	PAPER NUMBER
2666	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,144	RASHID ET AL.	
	Examiner	Art Unit	
	Michael J. Moore, Jr.	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-48,51-55,57-63,65-70,72 and 73* is/are rejected.

7)☒ Claim(s) *49,50,56,64 and 71* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Amendments made to claims **39, 41, 43, 44, and 52** to overcome the claim objections of the previous Office Action are proper and have been entered. These objections have been withdrawn.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **39-44, 46-48, 51-55, 57-63, 65-70, 72, and 73** are rejected under 35 U.S.C. 102(e) as being anticipated by Dai et al. (U.S. 6,658,016) ("Dai"). Dai teaches all of the limitations of the specified claims with the reasoning that follows.

Regarding *amended* claim **39**, "an apparatus" is anticipated by the packet switching fabric 10 (apparatus) shown in Figure 1.

"A set of input ports to receive data packets" is anticipated by network ports 14 shown in Figure 1 that transmit and receive data packets as spoken of on column 6, lines 26-36.

"A set of sink ports in communication with the set of input ports to receive and forward the data packets" is anticipated by data ring input ports 16 as well as control

ring input ports 22 of Figure 1 that receive data and control messages, respectively, as spoken of on column 6, lines 36-46.

"A set of data rings in communication with the set of input ports and the set of sink ports" is anticipated by the data ring 19 and the control ring 25 formed from the interconnection of the above mentioned ports and ring segments 18 and 24 of Figure 1, as spoken of on column 6, lines 49-51.

Lastly, "wherein one or more of the sink ports in the set of sink ports concurrently receives a plurality of data packets from two or more of the data rings" is anticipated by data ring input ports 16 as well as control ring input ports 22 of Figure 1 that receive messages from both data ring 19 and control ring 25, respectively, as spoken of on column 6, lines 36-51.

Regarding claim **40**, "wherein each packet in the plurality of data packets has a same destination address" is anticipated by the messages received by data ring input ports 16 as well as control ring input ports 22 of a switch 12 (destination) of Figure 1 as spoken of on column 6, lines 36-51.

Regarding claim **41**, "wherein each sink port in the set of sink ports includes a storage buffer that concurrently stores the plurality of data packets" is anticipated by data ring processing circuit 66 and control ring processing circuit 60 (buffers) of Figure 2A that receive messages via input ports 16 and 22 for subsequent processing.

Regarding claim **42**, "wherein the set of data rings couples each sink port in the set of sink ports to each input port in the set of input ports" is anticipated by data ring 19

and control ring 25 that couple data ring input ports 16 as well as control ring input ports 22 of Figure 1 to network ports 14 via switching elements 12.

Regarding claim **43**, "wherein a first sink port in the set of sink ports receives a first data packet in the plurality of data packets and a second data packet in the plurality of data packets" is anticipated by is anticipated by data ring input ports 16 as well as control ring input ports 22 of Figure 1 that receive data and control messages, respectively, as spoken of on column 6, lines 36-46.

Lastly, "a first input port in the set of input ports sources the first data packet" and "a second input port in the set of input ports sources at least a portion of the second data packet during a time when the first input port sources the first data packet" is anticipated by network ports 14 shown in Figure 1 that transmit and receive data packets (source) as spoken of on column 6, lines 26-36.

Regarding claim **44**, "wherein the first sink port receives the portion of the second data packet during a time the first sink port receives the first data packet" is anticipated by data ring input ports 16 as well as control ring input ports 22 of Figure 1 that receive data and control messages, respectively, as spoken of on column 6, lines 36-46.

Regarding claim **46**, "wherein each sink port in the set of sink ports snoops data packets on each data ring in the set of data rings" is anticipated by data ring processing circuit 66 and control ring processing circuit 60 of Figure 2A that receive messages via input ports 16 and 22 (sink ports) for subsequent processing.

Regarding claim **47**, "wherein the first sink port snoops data packets on each data ring in the set of data rings to determine whether the data packets are addressed

to a destination supported by the first sink port" is anticipated by data ring processing circuit 66 and control ring processing circuit 60 of Figure 2A that receive messages via input ports 16 and 22 (sink ports) for subsequent processing.

Regarding claim **48**, "wherein a first set of input ports in the set of input ports is coupled to a first data ring in the set of data rings and a second set of input ports in the set of input ports is coupled to a second data ring in the set of data rings, wherein the first set of input ports includes the first input port and the second set of input ports includes the second input port" is anticipated by data ring 19 and control ring 25 that couple data ring input ports 16 as well as control ring input ports 22 of Figure 1 to network ports 14 (input ports) via switching elements 12.

Regarding claim **51**, "wherein the apparatus is a crossbar switch" is anticipated by the packet switching fabric 10 (apparatus) shown in Figure 1.

Regarding claim **52**, "a set of input ports to receive data packets" is anticipated by input ports 88 shown in Figure 2A.

"A set of sink ports in communication with the set of input ports to receive and forward the data packets" is anticipated by output ports 84 of Figure 2A in communication with the input ports 88.

"A first sink port in the set of sink ports snoops data packets received by the set of input ports to determine whether the data packets are targeted to a destination supported by the first sink port" is anticipated by the data distribution unit 240 of Figure 3A that reads (snoops) the header information of the data burst received from the input

ports and then distributes the data bursts to appropriate output ports as spoken of on column 15, lines 35-45.

"The first sink port receives a first data packet and a second data packet" is anticipated by the two blocks of available space for accommodating two bursts of data packets (first and second data packets) at an output port as spoken of on column 21, lines 20-64.

Lastly, "the first sink port receives a portion of the second data packet at a time when the first sink port receives the first data packet" is anticipated by the reception of the first one or two bursts of data in a pipelined manner by an output port as spoken of on column 21, lines 20-65.

Regarding claim **53**, "wherein the first data packet is targeted to a first destination and the second data packet is targeted to the first destination" is anticipated by the two blocks of available space for accommodating two bursts of data packets (first and second data packets) at an output port as spoken of on column 21, lines 20-64.

Regarding claim **54**, "a first input port in the set of input ports sources the first data packet" is anticipated by input ports 88 sourcing a first data packet (control message from the control ring processing circuit) as spoken of on column 13, lines 30-61.

Lastly, "a second input port in the set of input ports sources a portion of the second data packet at a time when the first input port sources the first data packet" is anticipated by input ports 88 sourcing a second data packet (control message from the

control ring processing circuit) as spoken of on column 13, lines 63-67 as well as column 14, lines 1-35.

Regarding claim **55**, "a set of data rings in communication with the set of input ports and the set of sink ports" is anticipated by the data ring 16 and control ring 22 of Figure 2A in communication with input ports 88 as well as output ports 84.

Regarding claim **57**, "wherein the set of data rings couples each sink port in the set of sink ports to each input port in the set of input ports" is anticipated by data ring 16 and control ring 22 of Figure 2A in communication with input ports 88 as well as output ports 84.

Regarding claim **58**, "wherein each sink port in the set of sink ports snoops data packets on each data ring in the set of data rings" is anticipated by the data distribution unit 240 of Figure 3A that reads (snoops) the header information of the data burst received from the input ports as spoken of on column 15, lines 35-45.

Regarding claim **59**, "wherein the apparatus is a crossbar switch is anticipated by switching devices 12 of Figure 1.

Regarding claim **60**, "receiving a set of data packets" is anticipated by output ports 84 that receive data packets from data distribution control unit 240 as shown in Figure 3A and column 12, lines 63-67.

"Transferring the set of data packets to a set of data rings in communication with a set of sink ports" is anticipated by the packet routing and control unit 302 that transfers the data packet to the destination devices using the set of data rings as spoken of on column 14, lines 11-64.

"A sink port in the set of sink ports, determining whether to accept data packets in the set of data packets, based on a set of criteria" is anticipated by the data distribution unit 240 of Figure 3A that reads the header information of the data burst received from the input ports as spoken of on column 15, lines 35-45.

"The sink port collecting data for data packets accepted by the sink port" is anticipated by each output port having a buffer space for receiving bursts of data packets as spoken of on column 15, lines 45-55.

"The sink port collecting data for a first data packet" is anticipated by an output port receiving a first burst of packet data as spoken of on column 21, lines 20-65.

Lastly, "the sink port collecting data for a portion of a second data packet during a time period when the first data packet data is collected" is anticipated by the receiving of the first one or two bursts of data in a pipelined manner as spoken of on column 21, lines 20-65.

Regarding claim **61**, "wherein the first data packet and the second data packet are targeted to a first destination" is anticipated by the two blocks of available space for accommodating two bursts of data packets (first and second data packets) at an output port as spoken of on column 21, lines 20-64.

Regarding claim **62**, "receiving the first data packet" is anticipated by the output port receiving a first burst of data as spoken of on column 21, lines 20-65.

Lastly, "receiving a portion of the second data packet during a time period when the first data packet data is received" is anticipated by the receiving of the first one or two bursts of data in a pipelined manner as spoken of on column 21, lines 20-65.

Regarding claim **63**, "transferring the first data packet to a data ring in the set of data rings" is anticipated by one or two bursts of data being transferred from the source device to the destination device via the data ring as spoken of on column 21, lines 20-65.

Lastly, "transferring a portion of the second data packet to a data ring in the set of data rings during a time period when the first data packet data transfer is occurring" is anticipated by the transfer of data packets in a pipelined manner as spoken of on column 21, lines 20-65.

Regarding claim **65**, "the sink port issuing a rejection signal if the sink port determines not to accept the data packet, wherein the rejection signal terminates further reception of the data packet by the sink port" is anticipated by step 772 of Figure 10B where if a minimum amount of resources are not available, data transmission is stopped as spoken of on column 30, lines 60-67.

Regarding claim **66**, "the sink port transmitting the data packets collected" is anticipated by output ports 84 transmitting the data packets to appropriate destination devices as spoken of on column 8, lines 35-60.

Regarding claim **67**, "receiving a set of data packets on a set of input ports" is anticipated by the receiving of data packets by input ports 88 of Figure 3A as spoken of on column 13, lines 63-67 as well as column 14, lines 1-10.

"Receiving a first data packet" is anticipated by a first data burst received at the source device to be transmitted to the destination device as spoken of on column 21, lines 20-64.

"Receiving a second data packet" is anticipated by two data bursts received at the source device to be transmitted to the destination device as spoken of on column 21, lines 20-64.

"A sink port in a set of sink ports in communication with the set of input ports, determining whether to accept data packets in the set of data packets based on a set of criteria" is anticipated by the data distribution control unit coupled to the sink port that determines whether to accept data packets based upon header information as spoken of on column 15, lines 35-45.

"The sink port collecting data for data packets accepted by the sink port" is anticipated by each output port having a buffer space for receiving bursts of data as spoken of on column 15, lines 45-55.

"The sink port collecting data for the first data packet" is anticipated by an output port receiving a first burst of data as spoken of column 21, lines 20-65.

Lastly, "the sink port collecting data for a portion of the second data packet during a time period when the first data packet data collection is performed" is anticipated by the reception of first one or two bursts of data packets in a pipelined manner as spoken of on column 21, lines 20-65.

Regarding claim **68**, "wherein the first data packet and the second data packet are targeted to a first destination" is anticipated by the two blocks of available space for accommodating two bursts of data packets (first and second data packets) at an output port as spoken of on column 21, lines 20-64.

Regarding claim **69**, "wherein a portion of the second data packet is received during a time period when the first data packet reception is performed" is anticipated by the receiving of the first one or two bursts of data in a pipelined manner as spoken of on column 21, lines 20-65.

Regarding claim **70**, "transferring the first data packet to a data ring in the set of data rings" is anticipated by one or two bursts of data being transferred from the source device to the destination device via the data ring as spoken of on column 21, lines 20-65.

Lastly, "transferring a portion of the second data packet to a data ring in the set of data rings during a time period when the first data packet data transfer is occurring" is anticipated by the transfer of data packets in a pipelined manner as spoken of on column 21, lines 20-65.

Regarding claim **72**, "the sink port issuing a rejection signal if the sink port determines not to accept the data packet, wherein the rejection signal terminates further reception of the data packet by the sink port" is anticipated by step 772 of Figure 10B where if a minimum amount of resources are not available, data transmission is stopped as spoken of on column 30, lines 60-67.

Regarding claim **73**, "the sink port transmitting the data packets collected" is anticipated by output ports 84 transmitting the data packets to appropriate destination devices as spoken of on column 8, lines 35-60.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim **45** is rejected under 35 U.S.C. 103(a) as being unpatentable over Dai et al. (U.S. 6,658,016) ("Dai") in view of Yamamoto et al. (U.S. 6,392,991) ("Yamamoto").

Regarding claim **45**, Dai teaches the apparatus of claim **44**. Dai fails to teach wherein the set of data rings includes three data rings.

However, Yamamoto teaches a switching system in Figure 7 where a plurality of rings A, B, C, and D interconnect a plurality of switches.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the multiple ring architecture of Yamamoto with the switching system of Dai in order to provide efficient communication between various nodes as spoken of on column 4, lines 1-18 of Yamamoto.

Allowable Subject Matter

6. Claims **49, 50, 56, 64, and 71** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim **49**, Dai teaches the apparatus of claim **44**. Dai fails to teach where the first sink port snoops data packets on each data ring and determines whether to accept the first data packet based on the claimed criteria.

Regarding claim **50**, Dai teaches the apparatus of claim **44**. Dai fails to teach where the first sink port includes a ring interface a storage buffer and an output port that perform the claimed operations.

Regarding claim **56**, Dai teaches the apparatus of claim **55**. Dai fails to teach where the first sink port includes a ring interface a storage buffer and an output port that perform the claimed operations.

Regarding claim **64**, Dai teaches the method of claim **60**. Dai fails to teach where the sink port determines whether to accept the data packet by determining whether the sink port is enabled to receive data, determining whether the sink port has sufficient resources to store the data packet, determining whether the sink port is currently receiving a maximum allowable number of packets, and determining whether the data packet has a number of bytes within a predetermined range.

Regarding claim **71**, Dai teaches the method of claim **67**. Dai fails to teach where the sink port determines whether to accept the data packet by determining whether the sink port is enabled to receive data, determining whether the sink port has sufficient resources to store the data packet, determining whether the sink port is currently receiving a maximum allowable number of packets, and determining whether the data packet has a number of bytes within a predetermined range.

Response to Arguments

8. Applicant's arguments with respect to *amended* claims **39-48 and 51** have been considered but are moot in view of the new ground(s) of rejection provided above.

9. Applicant's arguments with respect to claims **52-55, 57-63, 65-70, 72, and 73** have been fully considered but they are not persuasive.

Regarding claim **52**, Applicant argues that *Dai* fails to teach or suggest a set of input ports to receive data packets, and a set of sink ports in communication with the set of input ports to receive and forward the data packets, where the first sink port receives a first and second data packet, and the first sink port receives a portion of the second data packet at a time when the first sink port receives the first data packet.

However, as provided above, *Dai* teaches output ports 84 of Figure 2A in communication with the input ports 88 as well as the reception of the first one or two bursts of data in a pipelined manner by an output port as spoken of on column 21, lines 20-65. This pipelining allows a sequence of packets to be received without waiting for individual acknowledgment over a certain "time period".

Giving a broadest reasonable interpretation of the term "time" in this limitation, it is held that this teaching anticipates the "first sink port receiving a portion of the second data packet at a time when the first sink port receives the first data packet."

Regarding claim **60**, Applicant argues that *Dai* fails to teach an apparatus having a set of data rings in communication with the set of sink ports within that apparatus.

However, based upon the claim language of claim **60**, it is held that the switching fabric 10 of Figure 1 of *Dai* can be construed broadly to be "an apparatus" comprising bidirectional ports 14 (input and sink ports) as well as data ring 19 and control ring 25 composed of ring segments.

Regarding claims **60 and 67**, Applicant also argues that *Dai* fails to teach an output port that collects data for a second data packet at approximately the same time as the output port collects data for a first data packet.

However, as provided above, *Dai* teaches output ports 84 of Figure 2A in communication with the input ports 88 as well as the reception of the first one or two bursts of data in a pipelined manner by an output port as spoken of on column 21, lines 20-65. This pipelining allows a sequence of packets to be received without waiting for individual acknowledgment over a certain "time period".

Giving a broadest reasonable interpretation of the term "time period" in this limitation, it is held that this teaching anticipates the "first sink port collecting data for a portion of a second data packet during a time period when step (d)(1) is being performed.

Regarding claims **53, 61, and 68,** Applicant argues that *Dai* does not teach a first data packet and a second data packet received by a single output port at approximately the same time being targeted to the same destination.

However, *Dai* teaches two blocks of available space for accommodating two bursts of data packets (first and second data packets) at an output port as spoken of on column 21, lines 20-64. This implies that data packets received by this output port have a same targeted destination, as these packets are both received by this output port. It is held that this teaching anticipates "wherein the first data packet is targeted to a first destination and the second data packet is targeted to the first destination".

Regarding claim **57**, Applicant argues that *Dai* fails to teach that the set of data rings couples each sink port in the set of sink ports to each input port in the set of input ports.

However, *Dai* teaches data ring 16 and control ring 22 of Figure 2A in communication with input ports 88 as well as output ports 84. These elements are coupled to each other as shown in Figure 1.

It is held that *Dai* anticipates this limitation.

Regarding claim **54**, Applicant argues that *Dai* fails to describe a single output port receiving first and second data packets sourced from a first input port and a second input port at approximately the same time.

However, *Dai* teaches input ports 88 sourcing a first and a second data packet (control message from the control ring processing circuit) as spoken of on column 13, lines 30-61.

It is held that *Dai* anticipates this limitation.

Regarding claims **62 and 69**, Applicant argues that *Dai* does not teach collecting data for more than one of the data bursts at the same time.

However, as provided above, *Dai* teaches output ports 84 of Figure 2A in communication with the input ports 88 as well as the reception of the first one or two bursts of data in a pipelined manner by an output port as spoken of on column 21, lines 20-65. This pipelining allows a sequence of packets to be received without waiting for individual acknowledgment over a certain "time period".

Giving a broadest reasonable interpretation of the term "time period" in this limitation, it is held that this teaching anticipates this limitation.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (571) 272-3168. The examiner can normally be reached on Monday-Friday (8:30am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael J. Moore, Jr.
Examiner
Art Unit 2666

mjm MM

Seema S. Rao 1/30/06
SEEMA S. RAO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600